The Amon patent is discussed in previous responses. Briefly, Amon discloses a parallel data structure and a dedicated Viterbi shift-left instruction which perform an add-compare-select operation. The Examiner asserts that the adding, subtracting, comparing and selecting operations of Amon are all carried out in the third single clock cycle. The Examiner cites Amon at column 2, lines 24-31 in which Amon describes:

> "adding a branch metric to the first path metric to obtain a first result; subtracting the branch metric from the second path metric to obtain a second result; comparing the first result to the second result, and selecting which is greater to become a first survivor metric, and refetching the first previous path metric during a third single clock cycle;".

A careful review indicates that Amon does not teach or suggest adding, subtracting, comparing and selecting operations carried out in a third single clock cycle. In fact, Amon teaches the following operations in the third single clock cycle.

> "comparing the first result to the second result, and selecting which is greater to become a first survivor metric, and refetching the first previous path metric during a third single clock cycle;"

The adding operation described by Amon is separated from the subtracting operation by a semicolon, and the subtracting operation of Amon is separated from the comparing, selecting and refetching operation by a semicolon. Thus, the adding and subtracting operations are separate operations and are not performed during the third single clock cycle. This conclusion is confirmed by the remainder of the Amon patent. Claim 7 at column 11, lines 6-40 of the Amon patent corresponds substantially with column 2, lines 18-39 of the Amon patent, except for additional limitations in the storing steps of claim 7. As indicated in claim 7, the comparing, selecting and refetching operations are performed during a third single clock cycle. The adding and subtracting operations are recited in separate paragraphs of claim 7 and thus are not performed in the third single clock cycle.

Amon discloses additional operations that are performed in a single clock cycle. Step 102 in Fig. 3 includes addition and loading an accumulator register in a single clock cycle (column 7, lines 39-53). Step 108 in Fig. 3 includes subtraction and loading an accumulator register in a single clock cycle (column 8, lines 39-47). Step 109 of Fig. 3 includes addition and loading a value into an accumulator register (column 8, lines 47-54). Assembly code for implementing the ACS butterfly in a digital signal processor is shown in the embodiments of Figs. 4 and 5 of Amon. Amon states that one loop of the ACS butterfly may be completed in 14 clock cycles according to the embodiment of Fig. 4 (column 9, lines 29-32). Amon further states that the number of clock cycles required to perform one loop of the ACS butterfly is reduced from 14 clock cycle to 10 clock cycles according to the embodiment of Fig. 5 (column 9, lines 41-46).

Amon describes additional operations that can be performed in a single clock cycle. Amon states that the Viterbi shift left instruction is executed within a single clock cycle (column 9, lines 61-64). Operations performed in a single clock cycle are also disclosed in claims 10, 12, 15 and 18 of Amon.

Notwithstanding the above disclosures, Amon does not teach or suggest a method for processing signal values in a digital signal processor *wherein adding, subtracting, comparing and selecting operations of a single trellis instruction are executed by the digital signal processor in a single clock cycle*, as recited in Applicants' claims 1 and 18. In every case, Amon requires multiple clock cycles to perform the operations of adding, subtracting, comparing and selecting of an ACS operation. Accordingly, claims 1 and 18 are clearly and patentably distinguished over Amon, and withdrawal of the rejection is respectfully requested.

Claims 2-6 depend from claim 1, and claims 25 and 26 depend from claim 18. Claims 2-6, 25 and 26 are patentable over Amon for at least the same reasons as claims 1 and 18.

Based upon the above discussion, claims 1-6, 18, 25 and 26 are in condition for allowance.

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: March 20, 2006

Respectfully submitted,

By William R. McClellan

William R. McClellan
Registration No.: 29,409
WOLF, GREENFIELD & SACKS, P.C.
Federal Reserve Plaza
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
(617) 646-8000

DD: 03/20/06